M52790SP/FP

AV Switch with I^{2}C Bus Control

REJ03F0187-0200
Rev.2.00
Sep 14, 2006

Description

The M52790 is AV switch semiconductor integrated circuit with I^{2}C bus control.

This IC contains 2-channels of 4-input audio switches and 2-channels of 4-input video switches. Each channel can be controlled independently.

The video switches contain amplifiers can be controlled a gain of output 0 dB or 6 dB.

Features

- Video and stereo sound switches in one package
- Wide frequency range (video switch): DC to 20 MHz
- High separation (video switch): Crosstalk –60 dB (Typ) at 1 MHz
- Two types of packages are provided: SDIP with a lead pitch of 1.778 mm (M52790SP); and SSOP with a lead pitch of 0.8 mm (M52790FP).

Application

Video equipment

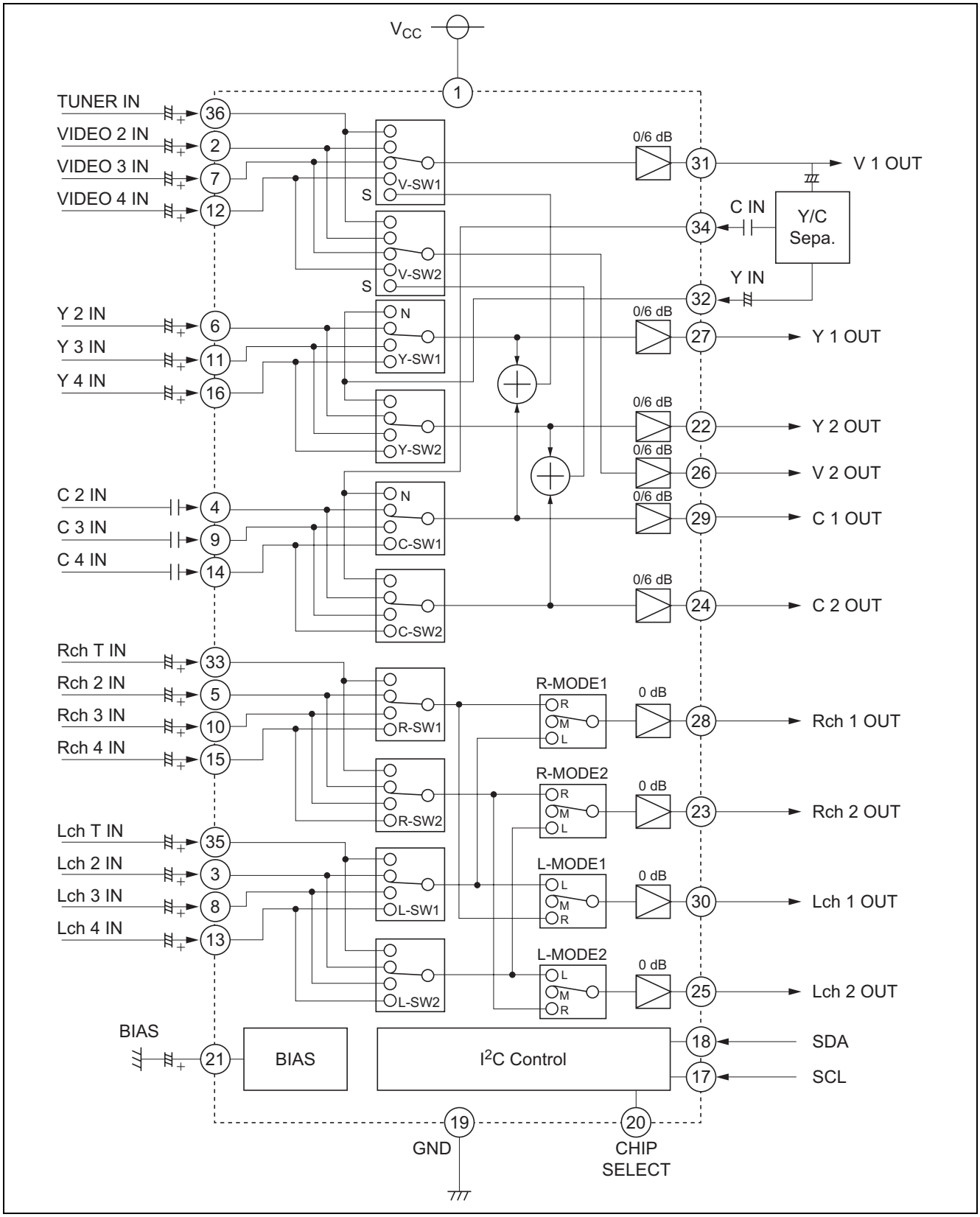
Recommended Operating Condition

Supply voltage: 4.7 V to 9.3 V

Rated supply voltage: 5 V, 9 V

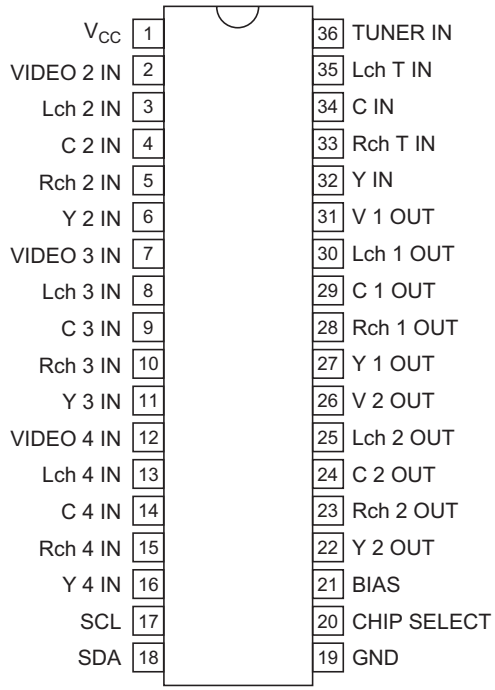
Maximum output current: 63 mA (at 9 V)

Block Diagram



Pin Arrangement

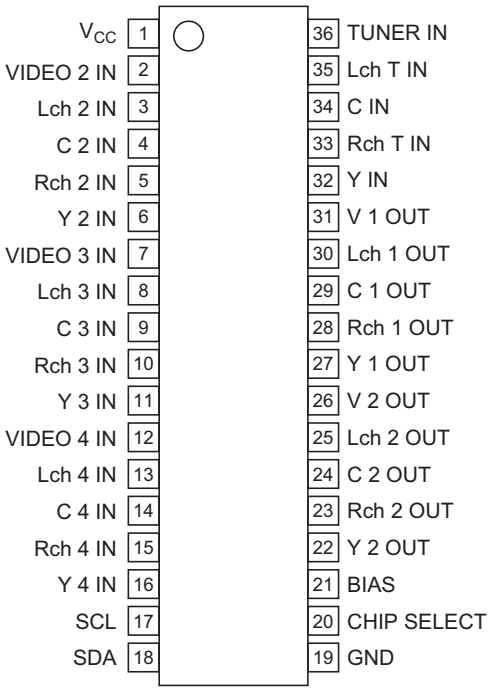
M52790SP



(Top view)

Outline: 36P4E
Lead pitch: 1.778 mm

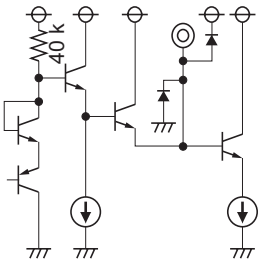
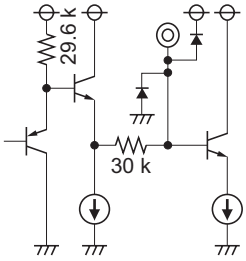
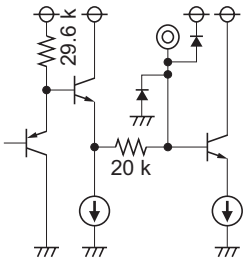
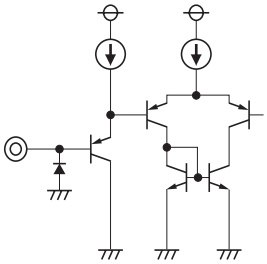
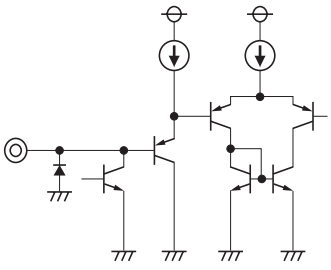
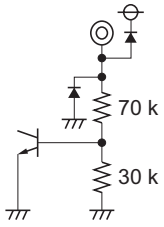
M52790FP

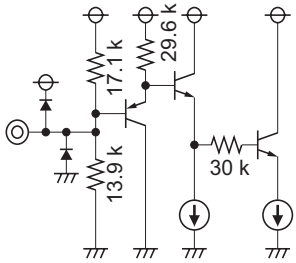
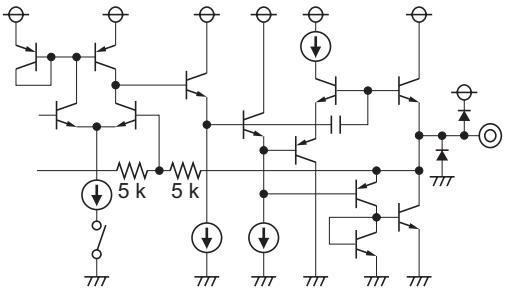
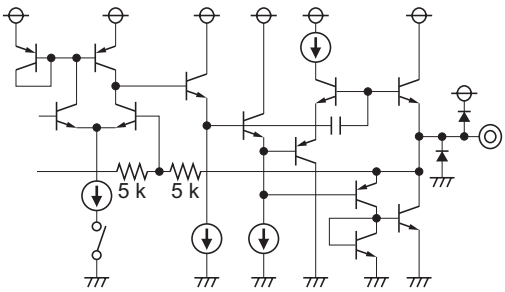
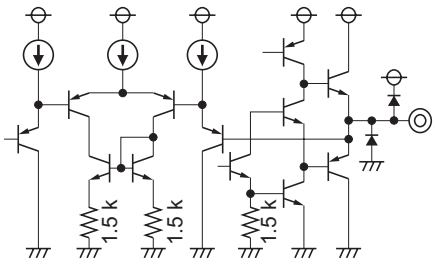


(Top view)

Outline: PRSP0036GA-B (36P2R-D)
Lead pitch: 0.8 mm

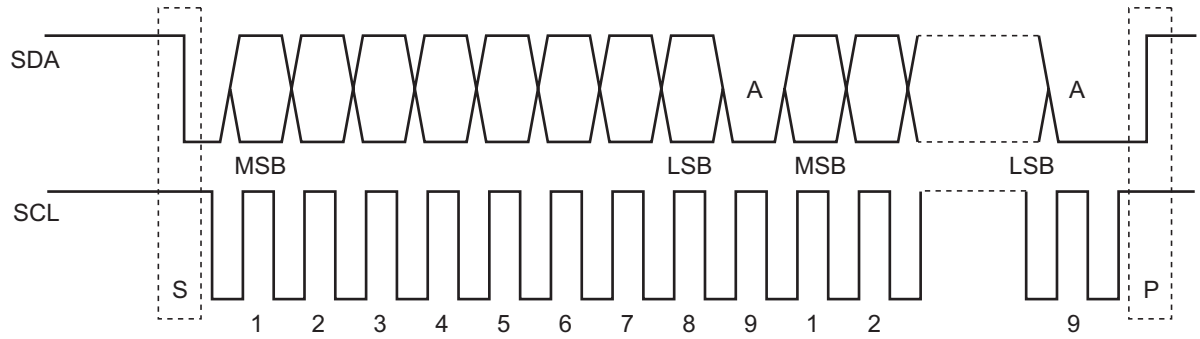
Pin Description

Pin No.	Name	Peripheral Circuit Pins	DC Voltage (V)	Remarks
1	V_{CC}	—	9 V	5 to 9 V
2 6 7 11 12 16 32 36	VIDEO 2 IN Y 2 IN VIDEO 3 IN Y 3 IN VIDEO 4 IN Y 4 IN Y IN TUNER IN		3.6 V	Clamp in
3 5 8 10 13 15 33 35	Lch 2 IN Rch 2 IN Lch 3 IN Rch 3 IN Lch 4 IN Rch 4 IN Rch T IN Lch T IN		4.7 V	
4 9 14 34	C 2 IN C 3 IN C 4 IN C IN		4.7 V	
17	SCL		V_{IL} max = 1.5 V V_{IH} min = 3.0 V	
18	SDA		V_{IL} max = 1.5 V V_{IH} min = 3.0 V V_{OL} max = 0.4 V	At Iin = 3 mA
19	GND	—	—	
20	CHIP SELECT		SLAVE ADDRESS 0 to 1.5 V: 90H 2.5 to V_{CC}: 92H OPEN: 90H	

Pin No.	Name	Peripheral Circuit Pins	DC Voltage (V)	Remarks
21	BIAS		4.2 V	
22 26 27 31	Y 2 OUT V 2 OUT Y 1 OUT V 1 OUT		SYNC CHIP DC = 2.9 V	
24 29	C 2 OUT C 1 OUT		4.0 V	
23 25 28 30	Rch 2 OUT Lch 2 OUT Rch 1 OUT Lch 1 OUT		4.0 V	

I²C Bus

I²C Bus (Inter IC Bus) is multi master bus system developed by PHILIPS. Two wires (SDA-serial data, SCL-serial clock) realize functions of start, stop, transferring data, synchronization and arbitration. The output stages of device connected to the bus must have an open drain or open collector in order to perform the wired-AND function.



Note: S: Start condition, a high to low transition of the SDA line while SCL is high
P: Stop condition, a low to high transition of the SDA line while SCL is high
A: Acknowledge

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Control

This IC controls 2-channel switches with 2-byte data (DATA1 and DATA2). SW1 is controlled by DATA1. SW2 is controlled by DATA2.

S	SLAVE ADDRESS	A	DATA1	A	DATA2	A	P

S: Start
A: Acknowledge
P: Stop

Slave address

1	0	0	1	0	0	X	0

R/W bit
Usually "0" (W: Master transmitter transmits to slave receiver)

Possible to select
20 pin High: 1, Low: 0

Data Byte Format

M52790 FUNCTION TABLE

S	SLAVE ADDRESS	A	DATA (D7 to D0)	A	DATA (DF to D8)	A	P

SLAVE ADDRESS

SLAVE ADDRESS	A6	A5	A4	A3	A2	A1	A0	R/W
	1	0	0	1	0	0	0/1	0

DATA1 (D7 to D0) CONT

DATA CONT	D7	D6	D5	D4	D3	D2	D1	D0
	AUDIO MODE1		—	Y/C AMP1	V AMP1	S/N	SW1 CONT	

VIDEO SW1 CONT

DATA			OUT		
S/N (S:1)	V-SW1				
D2	D1	D0	V OUT1	Y OUT1	C OUT1
0	0	0	T IN	Y IN	C IN
0	0	1	V 2 IN	Y IN	C IN
0	1	0	V 3 IN	Y IN	C IN
0	1	1	V 4 IN	Y IN	C IN
1	0	0	Y/C MIX T	Y IN	C IN
1	0	1	Y/C MIX 2	Y 2 IN	C 2 IN
1	1	0	Y/C MIX 3	Y 3 IN	C 3 IN
1	1	1	Y/C MIX 4	Y 4 IN	C 4 IN

AMP1 GAIN CONT

DATA	AMP	DATA	AMP
D4	YC AMP1	D3	V AMP1
0	0 dB	0	0 dB
1	6 dB	1	6 dB

AUDIO MODE1 CONT

DATA		MODE
D7	D6	
0	0	MUTE
0	1	R/R
1	0	L/L
1	1	NORMAL

AUDIO SW1 CONT

MODE		MUTE		R/R		L/L		NORMAL	
DATA		OUT		OUT		OUT		OUT	
D1	D0	Lch OUT 1	Rch OUT 1	Lch OUT 1	Rch OUT 1	Lch OUT 1	Rch OUT 1	Lch OUT 1	Rch OUT 1
0	0	MUTE	MUTE	Rch T IN	Rch T IN	Lch T IN	Lch T IN	Lch T IN	Rch T IN
0	1	MUTE	MUTE	Rch 2 IN	Rch 2 IN	Lch 2 IN	Lch 2 IN	Lch 2 IN	Rch 2 IN
1	0	MUTE	MUTE	Rch 3 IN	Rch 3 IN	Lch 3 IN	Lch 3 IN	Lch 3 IN	Rch 3 IN
1	1	MUTE	MUTE	Rch 4 IN	Rch 4 IN	Lch 4 IN	Lch 4 IN	Lch 4 IN	Rch 4 IN

DATA2 (DF to D8) CONT

DATA CONT	DF	DE	DD	DC	DB	DA	D9	D8
	AUDIO MODE2		—	Y/C AMP2	V AMP2	S/N	SW2 CONT	

VIDEO SW2 CONT

DATA			OUT		
S/N (S:1)	V-SW2				
DA	D9	D8	V OUT2	Y OUT2	C OUT2
0	0	0	T IN	Y IN	C IN
0	0	1	V 2 IN	Y 2 IN	C 2 IN
0	1	0	V 3 IN	Y 3 IN	C 3 IN
0	1	1	V 4 IN	Y 4 IN	C 4 IN
1	0	0	Y/C MIX T	Y IN	C IN
1	0	1	Y/C MIX 2	Y 2 IN	C 2 IN
1	1	0	Y/C MIX 3	Y 3 IN	C 3 IN
1	1	1	Y/C MIX 4	Y 4 IN	C 4 IN

AMP2 GAIN CONT

DATA	AMP	DATA	AMP
DC	Y/C AMP2	DB	V AMP2
0	0 dB	0	0 dB
1	6 dB	1	6 dB

AUDIO MODE2 CONT

DATA		MODE
DF	DE	
0	0	MUTE
0	1	R/R
1	0	L/L
1	1	NORMAL

AUDIO SW2 CONT

MODE		MUTE		R/R		L/L		NORMAL	
DATA		OUT		OUT		OUT		OUT	
D9	D8	Lch OUT 2	Rch OUT 2	Lch OUT 2	Rch OUT 2	Lch OUT 2	Rch OUT 2	Lch OUT 2	Rch OUT 2
0	0	MUTE	MUTE	Rch T IN	Rch T IN	Lch T IN	Lch T IN	Lch T IN	Rch T IN
0	1	MUTE	MUTE	Rch 2 IN	Rch 2 IN	Lch 2 IN	Lch 2 IN	Lch 2 IN	Rch 2 IN
1	0	MUTE	MUTE	Rch 3 IN	Rch 3 IN	Lch 3 IN	Lch 3 IN	Lch 3 IN	Rch 3 IN
1	1	MUTE	MUTE	Rch 4 IN	Rch 4 IN	Lch 4 IN	Lch 4 IN	Lch 4 IN	Rch 4 IN

Electrical Characteristics

(Ta = 25°C, V_{CC} = 9 V, unless otherwise noted)

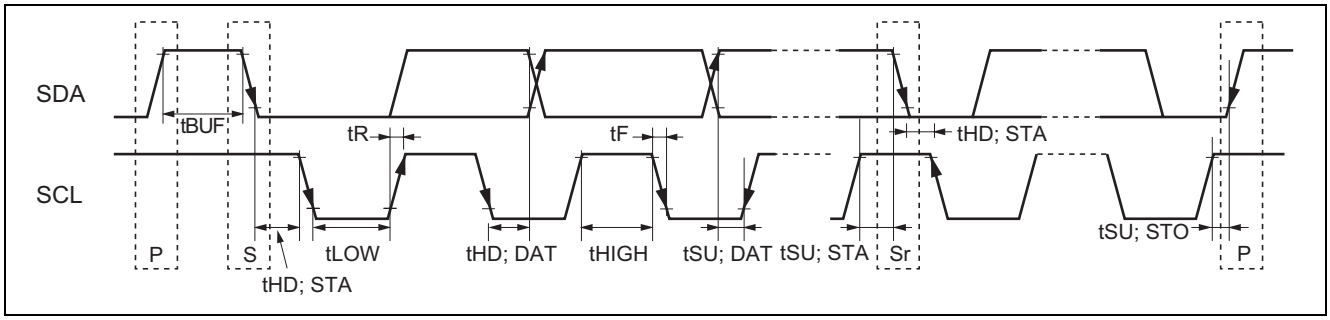
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Supply voltage	V_{CC}	4.7	—	9.3	V	
Circuit current	I_{CC}	—	63	83	mA	V_{CC} = 9 V, Vin = 0 Vp-p, Rl = ∞Ω
		—	54	71		V_{CC} = 5 V, Vin = 0 Vp-p, Rl = ∞Ω
Video						
Voltage gain	G	–0.5	0	0.5	dB	f = 100 kHz, 1 Vp-p (0 dB) (T→V_{1OUT})
		5.5	6	6.5		f = 100 kHz, 1 Vp-p (6 dB) (T→V_{1OUT})
		–0.5	0	0.5		f = 100 kHz, 1 Vp-p (0 dB) (Y→V_{1OUT})
		5.5	6	6.5		f = 100 kHz, 1 Vp-p (6 dB) (Y→V_{1OUT})
Frequency characteristics	F	–2.0	0	2.0	dB	f = 10 MHz/100 kHz, 1 Vp-p (0 dB) (T→V_{1OUT})
		–2.0	0	2.0		f = 10 MHz/100 kHz, 1 Vp-p (6 dB) (T→V_{1OUT})
		–2.0	0	2.0		f = 10 MHz/100 kHz, 1 Vp-p (0 dB) (Y→V_{1OUT})
		–2.0	0	2.0		f = 10 MHz/100 kHz, 1 Vp-p (6 dB) (Y→V_{1OUT})
Dynamic Range	D	4	—	—	Vp-p	V_{CC} = 9 V (0 dB) (T→V_{1OUT}) — f = 100 kHz Maximum with distortion <1.0%
		2	—	—		V_{CC} = 5 V (0 dB) (T→V_{1OUT})
		4	—	—		V_{CC} = 9 V (0 dB) (Y→V_{1OUT})
		2	—	—		V_{CC} = 5 V (0 dB) (Y→V_{1OUT})
Input impedance	Z_{IC}	14	20	26	kΩ	(C, C_2, C_3, C_4)
	Z_{IV}	—	—	—		Clamp in (T, V_2, V_3, V_4)
	Z_{IY}	—	—	—		Clamp in (Y, Y_2, Y_3, Y_4)
Crosstalk	CT	—	–60	–54	dB	f = 1 MHz, 1 Vp-p T→V_{1OUT} (at V_2 mode)
Audio						
Voltage gain	G	–0.5	0	0.5	dB	f = 1 kHz, 1 Vp-p (V_{CC} 9 V) (R_T→R_{1OUT})
		–0.5	0	0.5		f = 1 kHz, 1 Vp-p (V_{CC} 5 V) (R_T→R_{1OUT})
Frequency characteristics	F	–2.0	0	1	dB	f = 100 kHz/1 kHz, 1 Vp-p (R_T→R_{1OUT})
Total harmonic distortion	THD	—	0.01	0.05	%	f = 1 kHz, 2 Vp-p, at 400 Hz HPE + 30 kHz LPF (R_T→R_{1OUT})
Dynamic Range	D	5.5	6.0	—	Vp-p	f = 1 kHz, Maximum with distortion < 0.5% (R_T→R_{1OUT})
Output DC offset voltage	V_{OFF}	–20	0	20	mV	(MODE: R_T, R_2, R_3, R_4→R_{1OUT})
Input impedance	Z1	22	30	38	kΩ	(R_T, R_2, R_3, R_4, L_T, L_2, L_3, L_4)
Crosstalk	CT	—	–90	–84	dB	1 kHz, 1 Vp-p R_T→R_{1OUT} (at R_2 mode)
I^2C Bus control signal						
Max. input high voltage	V_{IH}	3.0	—	5.0	V	
Min. input low voltage	V_{IL}	0.0	—	1.5		
Low level output voltage (SDA)	V_{OL}	0.0	—	0.4		SDA = 3 mA
High level input current	I_{IH}	–10	—	10	μA	SDA, SCL = 4.5 V
Low level input current	I_{IL}	–10	—	10		SDA, SCL = 0.4 V
SCL clock frequency	f_{SCL}	0.0	—	100	kHz	
Time of bus must be free before a new transmission can start	t_{BUF}	4.7	—	—	μs	
Hold time at start condition	t_{HD};STA	4.0	—	—		
The low period of the clock	t_{LOW}	4.7	—	—		
The high period of the clock	t_{HIGH}	4.0	—	—		
Step-up time for start condition	t_{SU};STA	4.7	—	—		

Electrical Characteristics (cont.)

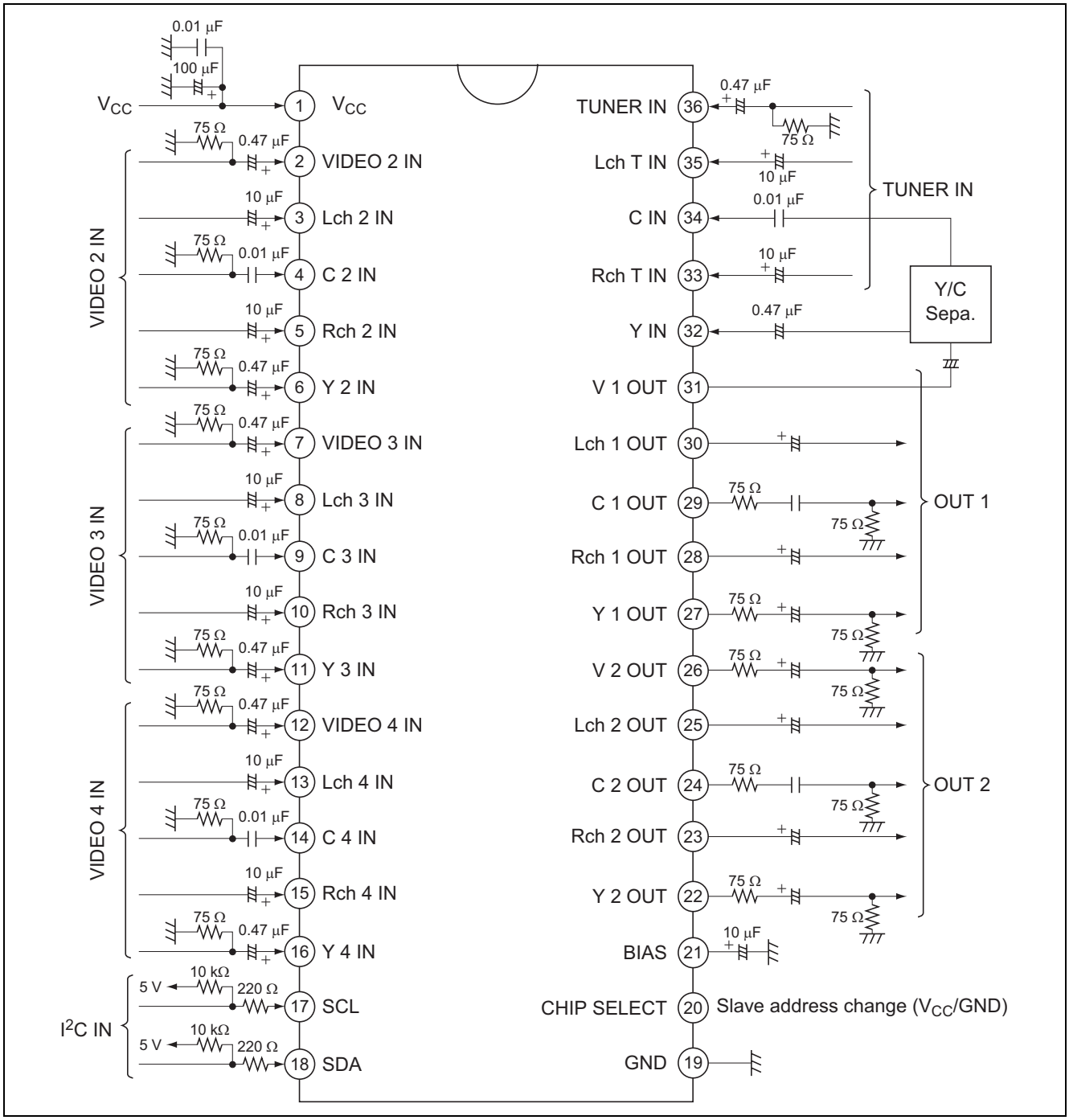
(Ta = 25°C, V_{CC} = 9 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Hold time DATA	t_{HD};DAT	5.0	—	—	ns	
Setup time DATA	t_{SU};DAT	250	—	—		
Rise time of both SDA and SCL line	t_R	—	—	1000		
Fall time of both SDA and SCL line	t_F	—	—	300		
Setup time for stop condition	t_{SU};STO	4.0	—	—	µs	

I²C Bus Control Signal



Application Circuit Example



Note How To Use This IC

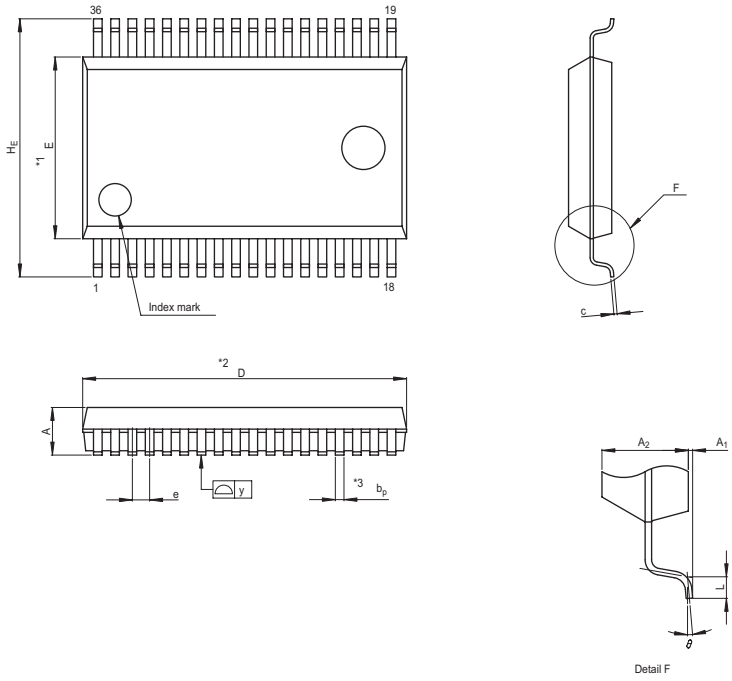
- Input signal with sufficient low impedance to input terminal.
- The capacitance of output terminal as small as possible.
- Set the capacitance between V_{CC} and GND near the pins if possible.
- Assign an area as large as possible for grounding.

Power-on Reset

- The M52790 has an internal power-on reset function that sets each control register to "0" during IC power ON.
- The power-on reset VTH has 2.5 V.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP36-8.4x15-0.80	PRSP0036GA-B	36P2R-D	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.8	15.0	15.2
E	8.2	8.4	8.6
A_2	—	2.05	—
A	—	—	2.35
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.10
L	0.3	0.5	0.7

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Colophon .6.0